1. A method of forming a metal oxide semiconductor field effect transistor (MOSFET) device on a semiconductor substrate comprising the steps of:

forming a gate insulator layer on said semiconductor substrate;

forming a conductive layer on said gate insulator layer;

forming a semiconductor layer on said conductive layer;

defining a conductive gate structure and an overlying semiconductor shape, on said gate insulator layer;

removing portion of said gate insulator layer not covered by said conductive gate structure;

forming a first doped region in an area of said semiconductor substrate not covered by said conductive gate structure;

forming composite insulator spacers on the sides of said conductive gate structure and on the sides of said semiconductor shape;

forming a second doped region in an area of said semiconductor substrate not covered by said conductive gate structure, or by said composite insulator spacers;

forming a metal layer;

performing an anneal procedure to form first metal silicide regions from an overlying first portion of said metal layer and from a top portion of said second doped region, and to form a second metal silicide region from an overlying second portion of said metal layer and from a portion of said semiconductor shape, while third portions

of said metal layer located on said composite insulator spacers remain unreacted; and

removing unreacted portions of said metal layer located on said composite insulator spacers.

2. The method of claim 1, wherein said MOSFET device is an N channel MOSFET device.

3. The method of claim 1, wherein said MOSFET device is a P channel MOSFET device.

4. The method of claim 1, wherein said MOSFET device is a complimentary metal oxide semiconductor (CMOS) device, comprised with both N channel and P channel MOSFET devices.

5. The method of claim 1, wherein said gate insulator layer is a high dielectric constant (high k) layer selected from a group consisting of silicon nitride, tantalum oxide, silicon oxynitride, zirconium oxide, hafnium oxide, aluminum oxide, all with a dielectric constant greater than 4.

6. The method of claim 1, wherein the thickness of said gate insulator layer is between about 15 to 500 Angstroms.

7. The method of claim 1, wherein said conductive layer is a refractory metal such as tungsten or molybdenum, obtained via physical vapor deposition procedures at a

thickness between about 800 to 2000 Angstroms.

8. The method of claim 1, wherein said semiconductor layer is an amorphous silicon layer, obtained at a thickness between about 200 to 1000 Angstroms, via a low pressure chemical vapor deposition (LPCVD), or via a plasma enhanced chemical vapor deposition (PECVD) procedure.

9. The method of claim 1, wherein said conductive gate structure and said overlying semiconductor shape are defined via an anisotropic reactive ion etch procedure using Cl_2 as an etchant for said semiconductor layer and for said conductive layer.

10. The method of claim 1, wherein said composite insulator spacers are comprised of an underlying silicon oxide shape at a thickness between about 50 to 250 Angstroms, and an overlying silicon nitride shape at a thickness between about 300 to 1000 Angstroms.

11. The method of claim 1, wherein said metal layer is selected from a group consisting of titanium, cobalt, nickel, zirconium, tantalum, or nickel - platinum, obtained via physical vapor deposition procedures at a thickness between about 50 to 500 Angstroms..

12. The method of claim 1, wherein said anneal procedure used to form metal silicide regions is a rapid thermal anneal procedure performed in an inert ambient at a temperature between about 450 to 900° C, for a time between about 30 to 400 sec.

13. The method of claim 1, wherein second metal silicide region is formed from a top portion of said semiconductor shape, leaving a bottom portion of said semiconductor shape located overlying said conductive gate structure.

14. The method of claim 1, wherein second metal silicide region located on said conductive gate structure, is formed consuming all of said semiconductor shape.

15. The method of claim 1, wherein unreacted portions of said metal layer are removed via a wet procedure using a solution comprised of HCl - H_2O_2 - NH_4OH - H_2SO_4.

16. A method of forming a MOSFET device on a semiconductor substrate featuring a metal silicide region on a metal gate structure, comprising the steps of:

forming a high dielectric constant (high k), gate insulator layer on said semiconductor substrate;

forming a first metal layer on said high k gate insulator layer;

forming an amorphous silicon layer on said first metal layer;

performing a first anisotropic reactive ion etch (RIE) procedure to define a metal gate structure and an overlying amorphous silicon shape, on said high k gate insulator layer;

removing portion of said high k gate insulator layer not covered by said metal gate structure;

forming a lightly doped source/drain region in an area of said semiconductor substrate not covered by said metal gate structure;

forming a silicon oxide layer;

forming a silicon nitride layer;

performing a second anisotropic RIE procedure to form composite insulator spacers comprised of an overlying silicon nitride shape and an underlying silicon oxide shape, on the sides of said metal gate structure and on the sides of said amorphous silicon shape;

forming a heavily doped source/drain region in an area of said semiconductor substrate not covered by said metal gate structure, or by said composite insulator spacers;

forming a second metal layer;

performing a first anneal procedure to form first metal silicide regions from an overlying first portion of said second metal layer and from a top portion of said heavily doped source/drain region, and to form a second metal silicide region from an overlying second portion of said metal layer and from a portion of said amorphous silicon shape, while a third portion of said second metal layer located on said composite insulator spacers remain unreacted;

removing unreacted third portion of said second metal layer; and

performing a second anneal procedure.

17. The method of claim 16, wherein said MOSFET device is an N channel MOSFET device.

18. The method of claim 16, wherein said MOSFET device is a P channel MOSFET device.

19. The method of claim 16, wherein said MOSFET device is a complimentary metal oxide semiconductor (CMOS) device, comprised with both N channel and P channel MOSFET devices.

20. The method of claim 16, wherein said high k gate insulator layer is selected from a group consisting of silicon nitride, tantalum oxide, silicon oxynitride, zirconium oxide, hafnium oxide, aluminum oxide.

21. The method of claim 16, wherein said high k gate insulator layer is comprised with a dielectric constant greater than 4, and at a thickness between about 15 to 150 Angstroms.

22. The method of claim 16, wherein said first metal layer is a refractory metal such as tungsten or molybdenum, obtained via physical vapor deposition procedures at a thickness between about 800 to 2000 Angstroms.

23. The method of claim 16, wherein said amorphous silicon layer is obtained at a thickness between about 200 to 1000 Angstroms, via a low pressure chemical vapor deposition (LPCVD), or via a plasma enhanced chemical vapor deposition (PECVD) procedure.

24. The method of claim 16, wherein said first anisotropic RIE procedure used to define said metal gate structure and said overlying amorphous silicon shape is performed using Cl_2 as an etchant.

25. The method of claim 16, wherein said silicon oxide layer is obtained via LPCVD or via PECVD procedures at a thickness between about 50 to 250 Angstroms

26. The method of claim 16, wherein said silicon nitride layer is obtained via LPCVD or via PECVD procedures a thickness between about 300 to 1000 Angstroms.

27. The method of claim 16, wherein said second metal layer is selected from a group consisting of titanium, cobalt, nickel, zirconium, tantalum, or nickel - platinum, obtained via physical vapor deposition procedures at a thickness between about 50 to 500 Angstroms.

28. The method of claim 16, wherein said first anneal procedure used to form metal silicide regions is a rapid thermal anneal (RTA) procedure performed in an inert ambient at a temperature between about 450 to 900° C, for a time between about 30 to 400 sec.

29. The method of claim 16, wherein second metal silicide region is formed from a top portion of said amorphous silicon shape, leaving an unreacted bottom portion of said amorphous silicon shape located overlying said metal gate structure.

30. The method of claim 16, wherein second metal silicide region located on said metal gate structure, is formed consuming all of said amorphous silicon shape.

31. The method of claim 16 wherein said unreacted portion of said third metal layer is removed via a wet procedure using a solution comprised of HCl - H_2O_2 - NH_4OH - H_2SO_4.